REMARKS

Applicant respectfully requests reconsideration of the present application in view of the foregoing amendments and in view of the reasons which follow.

Claims 1-24, 27, and 28 stand rejected. The Examiner has objected to claims 8 and 9. Claims 1, 8, 9, and 11 have been amended. Accordingly, claims 1-24, 27, and 28 are pending in the application.

The specification has been amended to update the cross reference to related applications. No new matter is added in the amendments to the specification.

As a preliminary matter, claims 8 and 9 have been amended in accordance with the Examiner's objection. No new matter is added in the amendments to the claims. Withdrawal of the objection to claims 8 and 9 is respectfully requested.

In paragraphs 2 and 3 of the Office Action, claims 1-3 and 7 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,350,311 (Chin). The Examiner states:

> Chin et al. discloses a method of manufacturing an integrated circuit, comprising; providing an amorphous semiconductor material 120 including germanium (see column 4, lines 36-39) above a bulk substrate of single crystal semiconductor material 100; annealing the amorphous semiconductor material (see column 4, lines 51-55) to form a single crystalline semiconductor layer 130 containing germanium; and doping the single crystalline semiconductor layer and the substrate at a source location and a drain location (see column 5, lines 1-5) to form a source region 160 and a drain region 160, whereby a channel region between the source region and the drain region includes a thin semiconductor germanium region (see figure 1E). Chin et al. also discloses providing a cap layer 140 before the doping step. A gate structure 150 is provided after the cap layer 140.

Applicant respectfully traverses the rejection.

With respect to independent claim 1, a laser annealing step is recited. Chin does not show, describe, or suggest such a laser annealing step. Indeed, Chin appears

to rely on a conventional rapid thermal annealing step and does not mention the use of laser annealing. Accordingly, withdrawal of the rejection of claim 1 and its dependent claims 2-11 is respectfully requested.

In paragraphs 4 and 5 of the Office Action, Claims 1-24 are rejected under 35 U.S.C. § 103 as being unpatentable over U.S. Patent No. 6,319,799 (Ouyang) in view of U.S. Patent No. 4,046,618 (Chaudhari). The Examiner states:

> Ouyang et al. discloses a process of forming a transistor with a silicon germanium channel region, the process comprising; depositing a thin silicon germanium material above a top surface of a semiconductor substrate forming a single crystalline silicon germanium material 30; depositing a thin silicon material above the single crystalline silicon germanium material forming single crystalline silicon material 34; and providing a source region and a drain region for the transistor, the source region and the drain region extending into the substrate (see figure 2B); providing an oxide layer 18 above the silicon material 34. Ouyang et al. also discloses forming silicide layers on the source and drain regions (see column 2, lines 29-35).
>
> Ouyang et al. is applied as above but lacks anticipation on forming the single crystalline layers by forming an amorphous material and annealing the amorphous material at a temperature between 1100-1400 degrees Celsius using an excimer laser with a 308 nanometers wavelength to forma single crystal layer; and disclosing the thickness of the layers.
>
> Chaudhari et al. discloses forming an amorphous layer on a silicon substrate and recrystallizing the amorphous layer by annealing to forma single crystalline layer. In view of this disclosure, it would have been obvious to a person having ordinary skills in the art at the time the invention was made to form the single crystalline layers in the primary reference of Ouyang et al. by forming an amorphous layer an recrystallizing the amorphous layer to form a single crystalline layer as disclose in Chaudhari et al. since this is a conventional process used to form single crystalline layers. Furthermore, optimizing the process disclosed by Ouyang et al. by suing a well-known method of forming a single crystalline layer is not considered to be patentable subject matter and its well within the level of a person having ordinary skills in the art.

Applicants respectfully traverse the rejection, Chin, Ouyang and Chaudhari are referred to below as the cited art.

Applicant respectfully submits that U.S. Patent No. 6,319,794 (Ouyang) is not prior art. Applicant has submitted herewith an affidavit from Bin Yu, the inventor listed in the present application, to remove Ouyang as prior art. The affidavit refers to an invention disclosure form that demonstrates that the subject matter of claims 1-10, 12-24, 27, and 28 was in the possession of the inventor before May 9, 2000. More specifically, the invention disclosure form shows that the subject matter of claims 1-10, 12-24, 27, and 28 was fully conceived by at least April 11, 2000 when it was received by the Assignee's technology law department. Thus, it is respectfully submitted that claims 1-10, 12-24, 27, and 28 are allowable over the cited art because Chin does not qualify as prior art under 35 U.S.C. § 102(e) based upon the Rule 131 declaration submitted herewith. Accordingly reconsideration and withdrawal of rejection of claims 1-10, 12-24, 27, and 28 under 35 U.S.C. § 103 in view of the cited art is respectfully requested.

With respect to dependent Claim 10, the limitations related to the depth of the silicide layer are recited. Claim 10 recites that the silicide layer has a depth greater than the second crystalline semiconductor layer. Such a configuration is not shown, described or suggested in the cited art. In Chin and Chaudhari, silicide layers are not even mentioned, much less the particular depth for the silicide with respect to another layer. In Ouyang, silicide layer and metal contacts 24 are not deeper than layer 30. In fact, silicide layers and metal contacts 24 are shown disposed entirely above layer 30. See Ouyang, Figure 1. Accordingly, it is respectfully submitted that Claim 11 is additionally patentable over the cited art.

Applicant believes that the present application is now in condition for allowance. Favorable reconsideration of the application as amended is respectfully requested.

The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

Respectfully submitted,

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By _____

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Version with Markings to Show Changes Made

In the Claims:

1. (Amended) A method of manufacturing an integrated circuit, comprising:

providing an amorphous semiconductor material including germanium above a bulk substrate of semiconductor material;

laser annealing the amorphous semiconductor material to form a single crystalline semiconductor layer containing germanium; and

doping the single crystalline semiconductor layer and the substrate at a source location and a drain location to form a source region and a drain region, whereby a channel region between the source region and the drain region includes a thin semiconductor germanium region.

8. (Amended) The method of claim 1, wherein the amorphous semiconductor [layer] material includes silicon germanium.

9. (Amended) The method of claim 7, wherein the amorphous semiconductor [layer] material includes silicon germanium.

11. (Amended) The method of claim [10] 1, further comprising

providing a second amorphous semiconductor material above the amorphous semiconductor material including germanium before the laser annealing step, wherein the laser annealing step forms a second single crystalline semiconductive layer from the second amorphous semiconductor material; and

siliciding the source region and the drain region to form a silicided layer wherein the depth of the silicided layer is deeper than the second single crystalline semiconductor layer

[wherein the annealing step is performed by an excimer laser].